DAILY ASSESSMENT REPORT

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| Date: | 04 June 2020 | Name: | Persis P |
| Course: | DIGITAL DESIGN USING HDL | USN: | 4AL17EC069 |
| Topic: | * Hardware modelling using   Verilog   * FPGA and ASIC Interview questions | Semester & Section: | 6th sem & B sec |
| GitHub  Repository: |  |  |  |

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| FORENOON SESSION DETAILS |
| Image of session |

Report

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Report can be typed or hand written for up to two pages.

Hardware modelling using

Verilog

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

Learnt about the Verilog hardware descri

ption language.



Understood the difference between behavioral and structural design styles.



Learnt to write test benches and analyze simulation results.



Learnt to model combinational and sequential circuits.

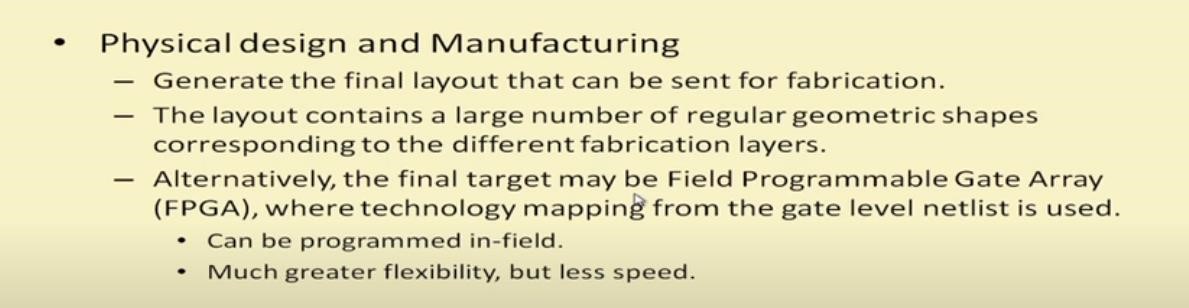
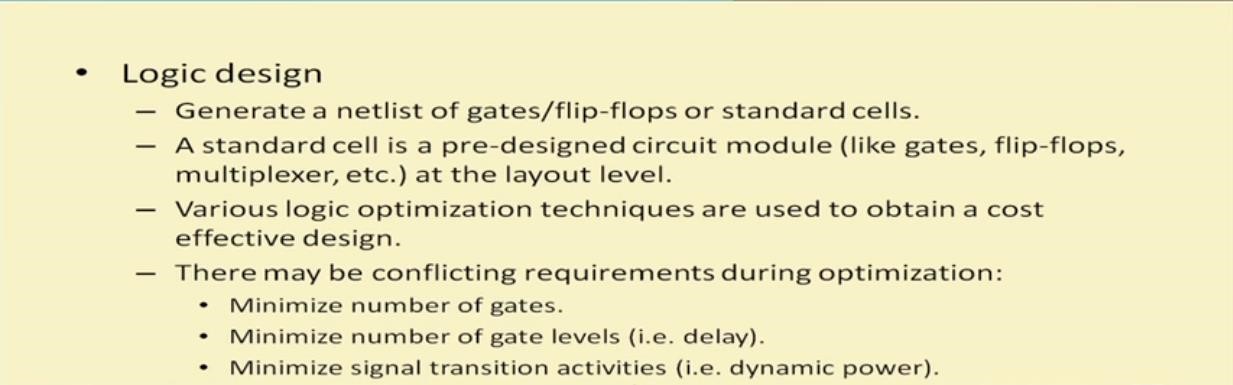


Distinguish between good and bad coding practices

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

Case studies with some complex designs.



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| FPGA and ASIC Interview questions:   Gone through the most frequently asked questions from Verilog in Interviews.      TASK: Implement a simple T Flipflop and test the module using a compiler.    Design: | | |
|  |  |  |
| module tff ( input clk, input rstn, input t, output reg q); |
| always @ (posedge clk) begin |
| if (!rstn) q <= 0; else if (t) q <= ~q; else q <= q; end endmodule |

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| Testbench:  module tb; reg clk; reg rstn; reg t; tff u0 ( .clk(clk),  .rstn(rstn),  .t(t),  .q(q));  always #5 clk = ~clk; | | | |
|  | | | |
| initial begin | | | |
| {rstn, clk, t} <= 0; | | | |
| $monitor ("T=%0t rstn=%0b t=%0d q=%0d", $time, rstn, t, q); repeat(2) @(posedge clk); rstn <= 1;  for (integer i = 0; i < 20; i = i+1) begin reg [4:0] dly = $random; #(dly) t <= $random; end #20 $finish; end endmodule | | | |
|  | | | |
| Date: | | 04 June 2020 | Name: | Persis P | |
| Course: | | The Python Mega Course | USN: | 4AL17EC069 | |
| Topic: | | Application 9: Build a Web-based Financial Graph | Semester & Section: | 6th sem & B sec | |

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| AFTERNOON SESSION DETAILS |
| Image of session:          Attended Bonus live session on “What is Electrical Engineering?” by Prof. S.Aniruddhan |

Report

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Web

-

based Financial Graph:



How to Download

Datasets with Python

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

Learnt analyzing

Stock Market Data

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

Plotting

Stock Market Data Candlestick Charts

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

Updating

Candlestick Charts with Bokeh Quadrants



Lear

nt to plot

Candlestick Charts with Bokeh Rectangles



Creating

Candlestick Segments



Stylizing the

obtained

Chart



Learnt t

he Concept Behind Embedding Bokeh



Sharing the

Charts in a Flask Webpage



Learnt how to Embed

the Bokeh Chart in a Webpage

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

Learnt to Dep

loy

the Chart Website to a Live Server

.



Below shown are the some pictures of graph produced, which are the stocks of Google

from 01 Jan 2020 to 30 May 2020 and

plotted using Candle

stick

format.

